SG1

Strain Gauge

Function Module

MODULE MANUAL

Revision History

Module Manual - SG1 Revision History		
Revision	**Revision Date**	**Description**
C	2022-10-11	EC0 C09714, transition to docbuilder format. Pg.5 thru 7, changed "Delta-Sigma" to "Sigma-Delta". Pg.6, remove FIR filter mode reference from Output Data Rate. Pg.7, added Status and Interrupts paragraph. Pg.13, changed Reset Min & Max Strain from R/W to W. Added Appendix: Pin-Out Details.

Module Manual - Status and Interrupts Revision History		
Revision	**Revision Date**	**Description**
C	2021-11-30	C08896; Transition manual to docbuilder format - no technical info change.

SG1 Measurement & Simulation Modules Strain Gauge Measurement Function Modules

4 Channels, Strain Gauge Measurement

Module SG1 is NAI's latest generation Strain Gauge Measurement Module. This intelligent, four-channel module is used on our Multifunction Embedded I/O Boards and Single Board Computers (SBCs).

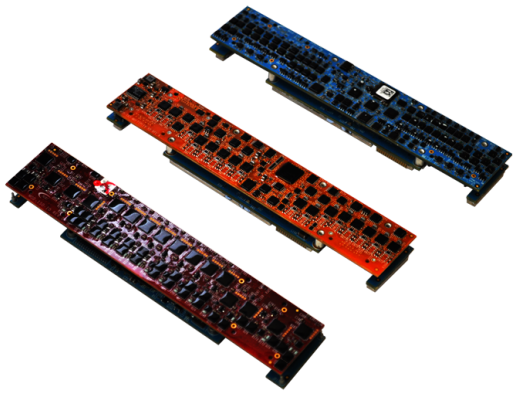
While there are several methods of measuring mechanical strain, the most common is with a strain gauge. The gauge provides electrical resistance that varies in proportion to the amount of strain in the device. The most widely used gauge is the bonded metallic strain gauge. To measure such small changes in resistance, strain gauges are almost always used in a bridge configuration with a voltage excitation source. The general Wheatstone bridge (conventional, 4-arm bridge) consists of four resistive arms with an excitation voltage, Vexc, that is applied across the bridge.

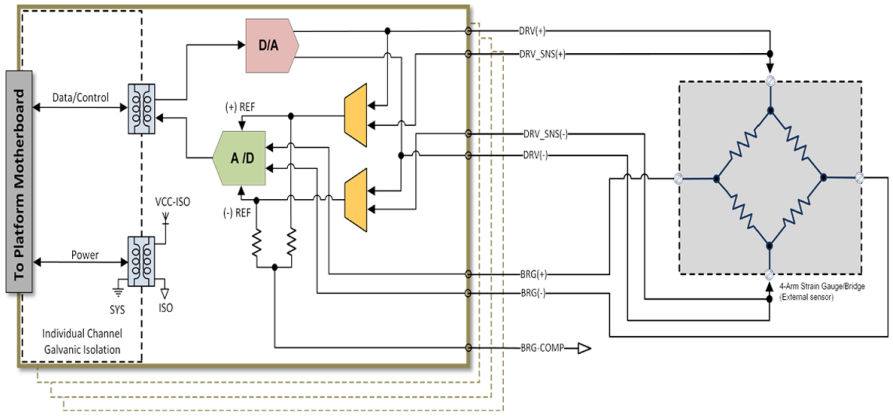
The SG1 module uses four independent, isolated input A/Ds. This module is designed to read output signals from a completed Wheatstone bridge (i.e., it can be used with one or more strain gauge elements as a completed 4-arm Wheatstone bridge) and is commonly used in applications requiring pressure, weight, and stress transducers interface/measurement. Each channel incorporates an Σ-Δ modulator, a PGA, and on-chip digital filtering intended for the measurement of wide dynamic range signals. Each channel also contains a fourth order digital filter, with several programmable filter options. When properly applied, the filter has deep notches at either 50 or 60 Hz.

The SG1 module provides a DC excitation, programmable from 2 - 12 VDC for interfacing to most load and accelerometer gauges.

The on-board processor/FPGA resources remove the user from the details of managing the A/D interface, register access, and sample timing. The processor firmware provides the user with a simpler user interface with high-level commands and post-calibration data. The module also contains internal factory calibration values stored in Flash. The SG1 automatically recalibrates for changes in reference voltage and die temperature.

Both internal and system calibration are included, providing the user with the option of removing only offset/gain errors internal to the A/Ds or the offset/gain errors of the complete end system.





Features

- **Four independent, isolated input A/Ds**
- **Designed to read output signals from a completed Wheatstone bridge**
- **Used in applications requiring pressure, weight, and stress transducers interface and measurement**
- **On-chip digital filtering for wide dynamic range signal measurement**
- **DC excitation for load and accelerometer gauge interface (programmable from 2-12 VDC)**
- **Onboard management of:**
  - **AD interface**
  - **Register access**
  - **Sample timing**
- **Internal and system calibration is included**

Specifications

Number of Channels	**4 differential input channels for load cell & accelerometer measurement.**
Input Interface	**Conventional 4-arm Wheatstone bridge, 4 or 6-wire interface.**
A/D Converter	**32-bit Sigma-Delta**
Output Resolution	**32-bit**
Accuracy	**± 0.1% Full-Scale (FS) range**
Digital Output	**Percent of Full Scale; Ratio (Vin/Vexc)**
Gain Settings	**1, 2, 4, 8, 16, and 32 (programmable)**
Input Impedance	**> 10 MΩ**
Input Coupling	**DC**
Bridge Excitation Voltage (Vexc)	**Independent Sources, Programmable 2 - 12 VDC**
Output Current (Maximum)	**100 mA / source**
Remote Voltage Sensing	**Yes**
Output Data Rate	**2.5 to 38,400 Hz (dependent on programmable filter settings).**
BIT (Built-in-Test)	**Continuous background "online" accuracy, open detection capability.**
ESD Protection	**Designed to meet the testing requirements of IEC 801-2 Level 2. (4 kV transient with a peak current of 7.5 A and a time constant of approximately 60 ns)**
Enhanced Functionality (pending)	**Each channel provided with: Programmable FFT with selectable sample rate and number of points (up to 64K). User selectable windowing function. Store value of unstrained voltage to include as compensation value**
Power	**5 VDC @ 850 mA typical (est.)**
Ground	**Channels isolated from each other and system ground.**
Weight	**1.5 oz. (42 g)**

Architected for Versatility

NAI's Configurable Open Systems Architecture™ (COSA®) offers a choice of over 100 smart I/O, communications, or Ethernet switch functions, providing the highest packaging density and greatest flexibility of ruggedized embedded product solutions in the industry. Preexisting, fully-tested functions can be combined in an unlimited number of ways quickly and easily.

One-Source Efficiencies

Eliminate man-months of integration with a configured, field-proven system from NAI. Specification to deployment is a seamless experience as all design, state-of-the-art manufacturing, assembly and test are performed - by one trusted source. All facilities are located within the U.S. and optimized for high-mix/low volume production runs and extended lifecycle support.

Product Lifecycle Management

From design to production and beyond, NAI's product lifecycle management strategy ensures the long-term availability of COTS products through configuration management, technology refresh and obsolescence component purchase and storage.

INTRODUCTION

This module manual provides information about the North Atlantic Industries, Inc. (NAI) Strain Gauge (SG) Measurement Function Module: SG1. This module is compatible with all latest generation NAI motherboards.

The SG1 provides four differential input channels for load cell & accelerometer measurement.

FEATURES

- Four independent, isolated input A/Ds
- Designed to read output signals from a completed Wheatstone bridge
- Used in applications requiring pressure, weight and stress transducers interface/measurement.
- On-chip digital filtering for wide dynamic range signal measurement
- DC excitation for load and accelerometer gauge interface (programmable from 2-12 VDC)
- Onboard management of A/D interface, register access and sample timing
- Internal and system calibration included

PRINCIPLE OF OPERATION

The SG1 module is NAI's latest generation Strain Gauge Measurement Module. This intelligent, four-channel module is used on our multifunction embedded boards and SBCs to provide load cell and accelerometer element measurement interfaces.

While there are several methods of measuring mechanical strain, the most common is with a strain gauge. The gauge provides electrical resistance that varies in proportion to the amount of strain in the device. The most widely used gauge is the bonded metallic strain gauge. To measure such small changes in resistance, strain gauges are almost always used in a bridge configuration with a voltage excitation source. The general Wheatstone bridge (conventional, 4-arm bridge) consists of four resistive arms with an excitation voltage, Vexc, that is applied across the bridge.

The SG1 module uses four independent, isolated input A/Ds. This module is designed to read output signals from a completed Wheatstone bridge (i.e., it can be used with one or more strain gauge elements as a completed 4-arm Wheatstone bridge) and is commonly used in applications requiring pressure, weight, and stress transducers interface/measurement. Each channel incorporates a Σ–Δ (Sigma-Delta) modulator, a PGA, and on-chip digital filtering intended for the measurement of wide dynamic range signals. Each channel also contains a fourth order digital filter, with several programmable filter options. When properly applied, the filter has deep notches at either 50 or 60 Hz.

The SG1 module provides a DC excitation, programmable from 2 – 12 VDC for interfacing to most load and accelerometer gauges.

The on-board processor/FPGA resources remove the user from the details of managing the A/D interface, register access, and sample timing. The processor firmware provides the user with a simpler user interface with high-level commands and post-calibration data. The module also contains internal factory calibration values stored in Flash.

Automatic Background Built-in Test (BIT)/Diagnostic Capability

Automatic background BIT testing is provided. Each channel is checked at periodic intervals for correct A/D operation. Any failure triggers an interrupt if enabled, with the results available in the status registers. The testing is transparent to the user and has no effect on the operation of this module.

Status and Interrupts

The SG Strain Gauge Measurement Module provide registers that indicate faults or events. Refer to "Status and Interrupts Module Manual" for the Principle of Operation description.

REGISTER DESCRIPTIONS

The register descriptions provide the Register Name, Type, Data Range, Read or Write information, power on default initialized values, a description of the function and a data table where applicable.

SG1 Measurement Registers

The SG1 measurement registers provide Vout/Vexc ratio measurements, strain measurements, and minimum/maximum strain readings.

Vout/Vexc

Function: Measures the ratio of the bridge output voltage to the excitation voltage.

Type: Single Precision Floating Point Value (IEEE-754)

Data Range: -1.0 to +1.0

Read/Write: R

Initialized Value: N/A

Operational Settings: Vout/Vexc measurement in V/V.

Vout/Vexc															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
D	D	D	D	D	D	D	D	D	D	D	**D**	**D**	**D**	**D**	**D**

Strain

Function: Measures the level of mechanical strain.

Type: Single Precision Floating Point Value (IEEE-754)

Data Range: -1000.0 to 1000.0

Read/Write: R

Initialized Value: N/A

Operational Settings: Strain is calculated based on the Vout/Vexc reading, bridge configuration type, nominal strain gauge resistance, gauge factor, Poisson ratio, and lead resistance. Units are in micro-strain (με).

Minimum Strain

Function: Stores the minimum strain level. When a new strain reading is lower than the value in this register, it will replace it.

Type: Single Precision Floating Point Value (IEEE-754)

Data Range: -1000.0 to 1000.0

Read/Write: R

Initialized Value: N/A

Operational Settings: Reset this value to zero by writing to the min/max reset register.

Maximum Strain

Function: Stores the maximum strain level. When a new strain reading is higher than the value in this register, it will replace it.

Type: Single Precision Floating Point Value (IEEE-754)

Data Range: -1000.0 to 1000.0

Read/Write: R

Initialized Value: N/A

Operational Settings: Reset this value to zero by writing to the min/max reset register.

SG1 Control Registers

The SG1 control registers provide the ability to configure the channels for the strain gauge interface and application.

Bridge Configuration Type

Function: Selects the bridge and strain gauge configuration.

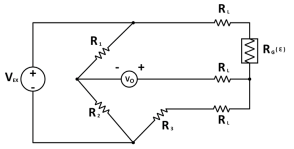
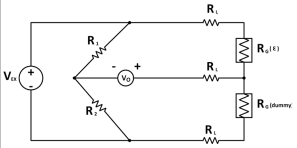
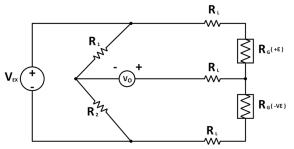
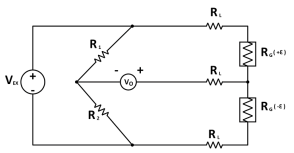
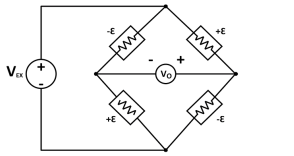
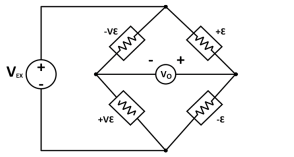
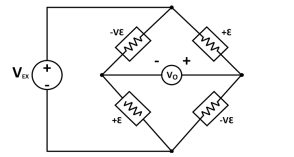
Type: unsigned binary word (32-bit)

Data Range: 0x0 to 0x6

Read/Write: R/W

Initialized Value: 0x0 (Quarter Bridge 1)

Operational Settings: See below table for compatible configurations.

Configuration Types	Register Value	Configuration Diagram	Strain Formula
Quarter-Bridge I	0x0		$\text{Strain } (\varepsilon) = \frac{-4V_r}{GF\,(1 + 2V_r)} \bullet \left[1 + \frac{R_L}{R_G}\right]$
Quarter-Bridge II	0x1		$\text{Strain } (\varepsilon) = \frac{-4V_r}{GF\,(1 + 2V_r)} \bullet \left[1 + \frac{R_L}{R_G}\right]$
Half-Bridge I	0x2		$\text{Strain } (\varepsilon) = \frac{-4V_r}{GF\,[(1 + \nu) - 2V_r\,(\nu-1)]} \bullet \left[1 + \frac{R_L}{R_G}\right]$
Half-Bridge II	0x3		$\text{Strain } (\varepsilon) = \frac{-2V_r}{GF} \bullet \left[1 + \frac{R_L}{R_G}\right]$
Full-Bridge I	0x4		$\text{Strain } (\varepsilon) = \frac{-V_r}{GF}$
Full-Bridge II	0x5		$\text{Strain } (\varepsilon) = \frac{-2V_r}{GF\,(\nu+1)}$
Full-Bridge III	0x6		$\text{Strain } (\varepsilon) = \frac{-2V_r}{GF\,[(\nu + 1) - V_r\,(\nu-1)]}$

PGA

Function: Sets the gain of the A/D.

Type: unsigned binary word (32-bit)

Data Range: 0x0 to 0x5 (See table)

Read/Write: R/W

Initialized Value: 0x2 (4V/V)

Operational Settings: Set the value based on the PGA table

PGA Register Value	Gain (V/V)
0x0	1
0x1	2
0x2	4
0x3	8
0x4	16
0x5	32

PGA															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0	0	0	0	0	**0**	**D**	**D**	**D**

Sample Rate

Function: Sets the sampling rate of the A/D.

Type: unsigned binary word (32-bit)

Data Range: 0x0 to 0xF (See table)

Read/Write: R/W

Initialized Value: 0x0 (2.5 SPS)

Operational Settings: Set the value based on Sample Rate table. Note: lower rates provide greater stability and accuracy in the readings. Per channel configuration.

Sample Rate Register Value	Sample Rate (SPS)	Bandwidth (Hz)
0x0	2.5	1.25
0x1	5	2.5
0x2	10	5
0x3	16.6666	8.3333
0x4	20	10
0x5	50	25
0x6	60	30
0x7	100	50
0x8	400	200
0x9	1200	600
0xA	2400	1200
0xB	4800	2400
0xC	7200	3600
0xD	14400	7200
0xE	19200	9600
0xF	38400	19200

Sample Rate															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0	0	0	0	0	**D**	**D**	**D**	**D**

Nominal Strain Gauge Resistance

Function: User defined resistance of the strain gauge in an unstrained condition.

Type: Single Precision Floating Point Value (IEEE-754)

Data Range: N/A

Read/Write: R/W

Initialized Value: 350.0 (programmed in ohms)

Operational Settings: Sets the user defined nominal strain gauge resistance to be used for strain calculation.

Gauge Factor

Function: User defined ratio of the fractional change in resistance to the fractional change in strain.

Type: Single Precision Floating Point Value (IEEE-754)

Data Range: N/A

Read/Write: R/W

Initialized Value: 2.0

Operational Settings: Sets the user defined gauge factor to be used for strain calculation.

Poisson Ratio

Function: User defined negative ratio of the strain in the transverse direction to the strain in the axial direction.

Type: Single Precision Floating Point Value (IEEE-754)

Data Range: N/A

Read/Write: R/W

Initialized Value: 0.3

Operational Settings: Sets the user defined Poisson ratio to be used for strain calculation.

Lead Resistance

Function: User defined resistance of the wires connecting the bridge to the module.

Type: Single Precision Floating Point Value (IEEE-754)

Data Range: N/A

Read/Write: R/W

Initialized Value: 0.0 (programmed in ohms)

Operational Settings: Sets the user defined lead resistance to be used for strain calculation.

Excitation Voltage

Function: User defined bridge excitation voltage.

Type: unsigned binary word (32-bit)

Data Range: 0x0 to 0xFFF (0.0V to 12V)

Read/Write: R/W

Initialized Value: 0x0 (off)

Operational Settings: Programmable bridge excitation voltage up to 12V. 12-bit value, LSB is calculated by 12V / (2^12 -1) and is approximately 2.93mV.

Excitation Voltage															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	D	D	D	D	D	D	D	**D**	**D**	**D**	**D**	**D**

Wire Select Mode

Function: Selects where to sense the excitation voltage. A 6-wire connection is required to sense the excitation voltage at the bridge. If the voltage sensing is done internally, only 4 wires are required.

Type: unsigned binary word (32-bit)

Data Range: 0x4, 0x6

Read/Write: R/W

Initialized Value: 0x4 (internal sensing)

Operational Settings: Set the Wire Measurement Mode as specified in the table.

Wire Select Mode Value	Description
0x4	4-wire configuration, internal sensing
0x6	6-wire configuration, remote sensing

Wire Select Mode															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0	0	0	0	0	0	**D**	**D**	**D**

Reset Minimum and Maximum Strain

Function: Resets the channel's minimum and maximum strain readings.

Type: unsigned binary word (32-bit)

Data Range: 0x0 to 0xF

Read/Write: W

Initialized Value: 0x0

Operational Settings: Writing a '1' resets the channel's minimum and maximum strain readings to 0.0. Bit-mapped by channel.

Reset Minimum and Maximum Strain															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0	0	0	0	0	**D**	**D**	**D**	**D**

Use Internal Bridge Completion

Function: Enables the bridge completion circuitry. When enabled, the user needs only to connect a half-bridge, and connect the bridge completion pin to the sense low pin.

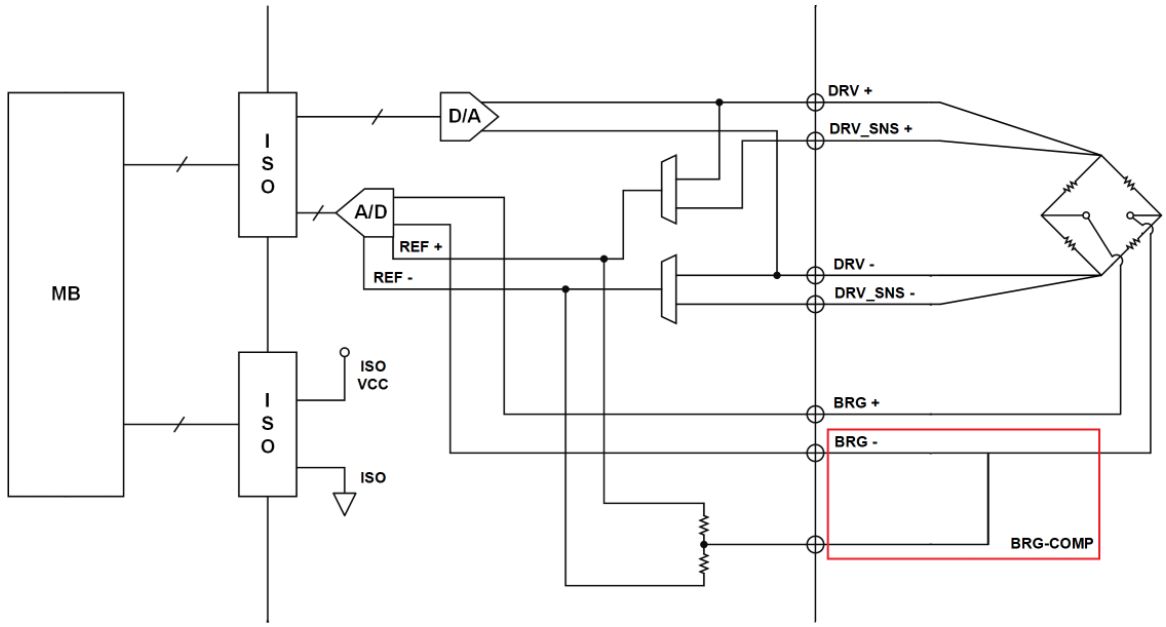
Type: unsigned binary word (32-bit)

Data Range: 0x0 to 0xF

Read/Write: R/W

Initialized Value: 0x0

Operational Settings: If configured with two arms of the Wheatstone bridge external to the module, the user must complete the bridge using the module's internal half-bridge. This is accomplished by wiring the BRG-COMP pin to the BRG - pin (as shown below).



Writing a '1' enables the bridge completion circuit for the channel. Bit-mapped per channel.

Use Internal Bridge Completion															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0	0	0	0	0	**D**	**D**	**D**	**D**

Strain Alert Detect Programming

The SG1 Strain Alert registers provide the ability to program four strain thresholds that will result in strain alerts.

Strain Alert Detect 1

A “low” and a “high” threshold value is specified for each strain threshold that will be used to set the Strain Alert statuses. The *Low Strain Alert 1* register sets the threshold value to use to set the *Low Strain Alert 1* status bit when the Strain reading is less than or equal to the low strain threshold value. Conversely, the *High Strain Alert 1* register sets the threshold values to use to set the *High Strain Alert 1* status bit when the Strain reading is greater than or equal to the high strain threshold value. These threshold values are individually configurable on a per channel basis.

Low Strain Alert 1

Function: Sets Low Strain Alert 1 value in micro-strain (με) for each channel.

Type: Single Precision Floating Point Value (IEEE-754)

Data Range: -1000.0 to 1000.0

Read/Write: R/W

Initialized Value: 0.0

Operational Settings: If the measured strain is less than or equal to the set value, then a *Low Strain Alert 1 Status* will be set. An interrupt will occur if the *Low Strain Alert 1 Interrupt Enable* register is set to **1**.

High Strain Alert 1

Function: Sets High Strain Alert 1 value in micro-strain (με) for each channel.

Type: Single Precision Floating Point Value (IEEE-754)

Data Range: -1000.0 to 1000.0

Read/Write: R/W

Initialized Value: 0.0

Operational Settings: If the measured strain is greater than or equal to the set value, then a *High Strain Alert 1 Status* will be set. An interrupt will occur if the *High Strain Alert 1 Interrupt Enable* register is set to **1**.

Strain Alert Detect 2

A “low” and a “high” threshold value is specified for each strain threshold that will be used to set the Strain Alert statuses. The *Low Strain Alert 2* register sets the threshold value to use to set the *Low Strain Alert 2* status bit when the Strain reading is less than or equal to the low strain threshold value. Conversely, the *High Strain Alert 2* register sets the threshold values to use to set the *High Strain Alert 2* status bit when the Strain reading is greater than or equal to the high strain threshold value. These threshold values are individually configurable on a per channel basis.

Low Strain Alert 2

Function: Sets Low Strain Alert 2 value in micro-strain (με) for each channel.

Type: Single Precision Floating Point Value (IEEE-754)

Data Range: -1000.0 to 1000.0

Read/Write: R/W

Initialized Value: 0.0

Operational Settings: If the measured strain is less than or equal to the set value, then a *Low Strain Alert 2 Status* will be set. An interrupt will occur if the *Low Strain Alert 2 Interrupt Enable* register is set to **1**.

High Strain Alert 2

Function: Sets High Strain Alert 2 value in micro-strain (με) for each channel.

Type: Single Precision Floating Point Value (IEEE-754)

Data Range: -1000.0 to 1000.0

Read/Write: R/W

Initialized Value: 0.0

Operational Settings: If the measured strain is greater than or equal to the set value, then a *High Strain Alert 2 Status* will be set. An interrupt will occur if the *High Strain Alert 2 Interrupt Enable* register is set to **1**.

Status and Interrupt Registers

The SG1 Module provides status registers for BIT, and Strain Alert.

BIT Loop Status

Function: This test represents the dynamic status of the BIT Loop test that checks the A/D interface and A/D operation health

Type: unsigned binary word (32-bit)

Data Range: 0x0000 0000 to 0x0000 000F

Read/Write: R

Initialized Value: 0

Operational Settings: The logic OR of this status along with the BIT Amp Status makes up the overall BIT status.

BIT Loop Status															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0	0	0	0	0	**Ch4**	**Ch3**	**Ch2**	**Ch1**

BIT Amp Status

Function: This test represents the dynamic status of the BIT Amp test that checks the front-end circuitry of the channel

Type: unsigned binary word (32-bit)

Data Range: 0x0000 0000 to 0x0000 000F

Read/Write: R

Initialized Value: 0

Operational Settings: The logic OR of this status along with the BIT Loop Status makes up the overall BIT status

BIT Amp Status															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0	0	0	0	0	**Ch4**	**Ch3**	**Ch2**	**Ch1**

BIT Status

There are four registers associated with the BIT Status: *Dynamic, Latched, Interrupt Enable,* and *Set Edge/Level Interrupt*.

BIT Dynamic Status															
BIT Latched Status															
BIT Interrupt Enable															
BIT Set Edge/Level Interrupt															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0	**0**	**0**	**0**	**0**	**Ch4**	**Ch3**	**Ch2**	**Ch1**

Function: Indicates the corresponding channel BIT status or configuration

Type: unsigned binary word (32-bit)

Data Range: 0x0000 0000 to 0x0000 000F

Read/Write: R (*Dynamic*), R/W (*Latched*, *Interrupt Enable*, *Edge/Level Interrupt*)

Initialized Value: 0

Strain Alert Status

There are four registers associated with each of the Strain Alert Statuses: *Dynamic, Latched, Interrupt Enable,* and *Set Edge/Level Interrupt*.

Strain Alert Low 1 Dynamic Status															
Strain Alert Low 1 Latched Status															
Strain Alert Low 1 Interrupt Enable															
Strain Alert Low 1 Set Edge/Level Interrupt															
Strain Alert High 1 Dynamic Status															
Strain Alert High 1 Latched Status															
Strain Alert High 1 Interrupt Enable															
Strain Alert High 1 Set Edge/Level Interrupt															
Strain Alert Low 2 Dynamic Status															
Strain Alert Low 2 Latched Status															
Strain Alert Low 2 Interrupt Enable															
Strain Alert Low 2 Set Edge/Level Interrupt															
Strain Alert High 2 Dynamic Status															
Strain Alert High 2 Latched Status															
Strain Alert High 2 Interrupt Enable															
Strain Alert High 2 Set Edge/Level Interrupt															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0	0	0	0	0	**Ch4**	**Ch3**	**Ch2**	**Ch1**

Function: Sets the corresponding bit associated with the channel's Strain Alert indication for strain readings that are below or above the associated thresholds.

Type: unsigned binary word (32-bit)

Data Range: 0x0000 0000 to 0x0000 000F

Read/Write: R (*Dynamic*), R/W (*Latched*, *Interrupt Enable*, *Edge/Level Interrupt*)

Initialized Value: 0

Error Summary Status

There are four registers associated with the Summary Status: *Dynamic, Latched, Interrupt Enable,* and *Set Edge/Level Interrupt.*

Summary Status Dynamic Status															
Summary Status Latched Status															
Summary Status Interrupt Enable															
Summary Status Set Edge/Level Interrupt															
D31	**D30**	**D29**	**D28**	**D27**	**D26**	**D25**	**D24**	**D23**	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	0	0	0	0	0	0	**Ch4**	**Ch3**	**Ch2**	**Ch1**

Function: Sets the corresponding bit when a fault is detected for BIT on that channel.

Type: unsigned binary word (32-bit)

Data Range: 0x0000 0000 to 0x0000 000F

Read/Write: R (*Dynamic*), R/W (*Latched*, *Interrupt Enable*, *Edge/Level Interrupt*)

Initialized Value: 0

Summary Events Table

Module	BIT	Overcurrent	External Power Loss	Open Line	External Power Under Volt	External Power Over Volt	Over Temp	Surge Suppressor Fault
SG1	X							

Interrupt Vector and Steering

When interrupts are enabled, the interrupt vector associated with the specific interrupt can be programmed (typically with a unique number/identifier) such that it can be utilized in the Interrupt Service Routine (ISR) to identify the type of interrupt. When an interrupt occurs, the contents of the Interrupt Vector registers is reported as part of the interrupt mechanism.

In addition to specifying the interrupt vector, the interrupt can be directed (“steered”) to the native bus or to the application running on the onboard ARM processor.

Note, the Interrupt Vector and Interrupt Steering registers are mapped to the Motherboard Common Memory and these registers are associated with the Module Slot position (refer to Function Register Map).

Interrupt Vector

Function: Set an identifier for the interrupt.

Type: unsigned binary word (32-bit)

Data Range: 0 to 0xFFFF FFFF

Read/Write: R/W

Initialized Value: 0

Operational Settings: When an interrupt occurs, this value is reported as part of the interrupt mechanism.

Interrupt Steering

Function: Sets where to direct the interrupt.

Type: unsigned binary word (32-bit)

Data Range: See Table

Read/Write: R/W

Initialized Value: 0

Operational Settings: When an interrupt occurs, the interrupt is sent as specified:

Direct Interrupt to VME	1
Direct Interrupt to ARM Processor (via SerDes) *(Custom App on ARM or NAI Ethernet Listener App)*	2
Direct Interrupt to PCIe Bus	5
Direct Interrupt to cPCI Bus	6

FUNCTIONAL REGISTER MAP

Key: ***Bold Italic = Configuration/Control***

Bold Underline = Measurement/Status

*When an event is detected, the bit associated with the event is set in this register and will remain set until the user clears the event bit. Clearing the bit requires writing a 1 back to the specific bit that was set when read (i.e. write-1-to-clear, writing a '1' to a bit set to '1' will set the bit to '0').

~ Data is always in Floating Point.

SG1 Measurement Registers

0x2034	**Vout/Vexe Ch 1~**	R
0x2134	**Vout/Vexe Ch 2~**	R
0x2234	**Vout/Vexe Ch 3~**	R
0x2334	**Vout/Vexe Ch 4~**	R

0x2038	**Strain (με) Ch 1~**	R
0x2138	**Strain (με) Ch 2~**	R
0x2238	**Strain (με) Ch 3~**	R
0x2338	**Strain (με) Ch 4~**	R

0x203C	**Minimum Strain (με) Ch 1~**	R
0x213C	**Minimum Strain (με) Ch 2~**	R
0x223C	**Minimum Strain (με) Ch 3~**	R
0x233C	**Minimum Strain (με) Ch 4~**	R

0x2040	**Maximum Strain (με) Ch 1~**	R
0x2140	**Maximum Strain (με) Ch 2~**	R
0x2240	**Maximum Strain (με) Ch 3~**	R
0x2340	**Maximum Strain (με) Ch 4~**	R

SG1 Control Registers

0x2000	***Bridge Configuration Type Ch 1***	R/W
0x2100	***Bridge Configuration Type Ch 2***	R/W
0x2200	***Bridge Configuration Type Ch 3***	R/W
0x2300	***Bridge Configuration Type Ch 4***	R/W

0x2044	***PGA Ch 1***	R/W
0x2144	***PGA Ch 2***	R/W
0x2244	***PGA Ch 3***	R/W
0x2344	***PGA Ch 4***	R/W

0x201C	***Sample Rate Ch 1***	R/W
0x211C	***Sample Rate Ch 2***	R/W
0x221C	***Sample Rate Ch 3***	R/W
0x231C	***Sample Rate Ch 4***	R/W

0x2004	***Nominal Strain Gauge Resistance Ch 1***	R/W
0x2104	***Nominal Strain Gauge Resistance Ch 2***	R/W
0x2204	***Nominal Strain Gauge Resistance Ch 3***	R/W
0x2304	***Nominal Strain Gauge Resistance Ch 4***	R/W

0x2008	***Gauge Factor Ch 1***	R/W
0x2108	***Gauge Factor Ch 2***	R/W
0x2208	***Gauge Factor Ch 3***	R/W
0x2308	***Gauge Factor Ch 4***	R/W

0x200C	***Poisson Ratio Ch 1***	R/W
0x210C	***Poisson Ratio Ch 2***	R/W
0x220C	***Poisson Ratio Ch 3***	R/W
0x230C	***Poisson Ratio Ch 4***	R/W

0x2010	***Lead Resistance Type Ch 1***	R/W
0x2110	***Lead Resistance Type Ch 2***	R/W
0x2210	***Lead Resistance Type Ch 3***	R/W
0x2310	***Lead Resistance Type Ch 4***	R/W

0x2014	***Excitation Voltage Ch 1***	R/W
0x2114	***Excitation Voltage Ch 2***	R/W
0x2214	***Excitation Voltage Ch 3***	R/W
0x2314	***Excitation Voltage Ch 4***	R/W

0x2018	***4-Wire/6-Wire Select Ch 1***	R/W
0x2118	***4-Wire/6-Wire Select Ch 2***	R/W
0x2218	***4-Wire/6-Wire Select Ch 3***	R/W
0x2318	***4-Wire/6-Wire Select Ch 4***	R/W

0x1000	***Reset Minimum and Maximum Strain Ch 1-4***	R/W

0x1004	***Use Internal Bridge Completion Ch 1-4***	R/W

Strain Alert Detect Programming Registers

0x2028	***Low Strain Alert 1 Ch 1~***	R
0x2128	***Low Strain Alert 1 Ch 2~***	R
0x2228	***Low Strain Alert 1 Ch 2~***	R
0x2328	***Low Strain Alert 1 Ch 2~***	R

0x202C	***Low Strain Alert 2 Ch 1~***	R
0x212C	***Low Strain Alert 2 Ch 2~***	R
0x222C	***Low Strain Alert 2 Ch 2~***	R
0x232C	***Low Strain Alert 2 Ch 2~***	R

0x2020	***High Strain Alert 1 Ch 1~***	R
0x2120	***High Strain Alert 1 Ch 2~***	R
0x2220	***High Strain Alert 1 Ch 2~***	R
0x2320	***High Strain Alert 1 Ch 2~***	R

0x2024	***High Strain Alert 2 Ch 1~***	R
0x2124	***High Strain Alert 2 Ch 2~***	R
0x2224	***High Strain Alert 2 Ch 2~***	R
0x2324	***High Strain Alert 2 Ch 2~***	R

Status Registers

0x1100	***BIT Loop Status Ch 1-4***	R/W

0x1104	***BIT Amp Status Ch 1-4***	R/W

BIT Registers

0x0800	**Dynamic Status**	R
0x0804	**Latched Status***	R/W
0x0808	***Interrupt Enable***	R/W
0x080C	***Set Edge/Level Interrupt***	R/W

Status Registers

High Strain Alert 1

0x0820	**Dynamic Status**	R
0x0824	**Latched Status***	R/W
0x0828	***Interrupt Enable***	R/W
0x082C	***Set Edge/Level Interrupt***	R/W

High Strain Alert 2

0x0830	**Dynamic Status**	R
0x0834	**Latched Status***	R/W
0x0838	***Interrupt Enable***	R/W
0x083C	***Set Edge/Level Interrupt***	R/W

Low Strain Alert 1

0x0840	**Dynamic Status**	R
0x0844	**Latched Status***	R/W
0x0848	***Interrupt Enable***	R/W
0x084C	***Set Edge/Level Interrupt***	R/W

Low Strain Alert 2

0x0850	**Dynamic Status**	R
0x0854	**Latched Status***	R/W
0x0858	***Interrupt Enable***	R/W
0x085C	***Set Edge/Level Interrupt***	R/W

Error Summary

0x09A0	**Dynamic Status**	R
0x09A4	**Latched Status***	R/W
0x09A8	***Interrupt Enable***	R/W
0x09AC	***Set Edge/Level Interrupt***	R/W

Interrupt Registers

The Interrupt Vector and Interrupt Steering registers are located on the Motherboard Memory Space and do not require any Module Address Offsets. These registers are accessed using the absolute addresses listed in the table below.

0x0500	***Module 1 Interrupt Vector 1 - BIT***	R/W
0x0504	***Module 1 Interrupt Vector 2 - Reserved***	R/W
0x0508	***Module 1 Interrupt Vector 3 - Strain Alert Low 1***	R/W
0x050C	***Module 1 Interrupt Vector 4 - Strain Alert Low 2***	R/W
0x0510	***Module 1 Interrupt Vector 5 - Strain Alert High 1***	R/W
0x0514	***Module 1 Interrupt Vector 6 - Strain Alert High 2***	R/W
0x0518 to 0x0564	***Module 1 Interrupt Vector 7-26 - Reserved***	R/W
0x0568	***Module 1 Interrupt Vector 27 - Summary***	R/W
0x056C to 0x057C	***Module 1 Interrupt Vector 28-32 - Reserved***	R/W

0x0600	***Module 1 Interrupt Steering 1 - BIT***	R/W
0x0604	***Module 1 Interrupt Steering 2 - Reserved***	R/W
0x0608	***Module 1 Interrupt Steering 2 - Strain Alert Low 1***	R/W
0x060C	***Module 1 Interrupt Steering 3 - Strain Alert Low 2***	R/W
0x0610	***Module 1 Interrupt Steering 4 - Strain Alert High 1***	R/W
0x0614	***Module 1 Interrupt Steering 5 - Strain Alert High 2***	R/W
0x0618 to 0x0664	***Module 1 Interrupt Steering 6-26 - Reserved***	R/W
0x0668	***Module 1 Interrupt Steering 27 - Summary***	R/W
0x066C to 0x067C	***Module 1 Interrupt Steering 28-32 - Reserved***	R/W

0x0700	***Module 2 Interrupt Vector 1 - BIT***	R/W
0x0704	***Module 2 Interrupt Vector 2 - Reserved***	R/W
0x0708	***Module 2 Interrupt Vector 3 - Strain Alert Low 1***	R/W
0x070C	***Module 2 Interrupt Vector 4 - Strain Alert Low 2***	R/W
0x0710	***Module 2 Interrupt Vector 5 - Strain Alert High 1***	R/W
0x0714	***Module 2 Interrupt Vector 6 - Strain Alert High 2***	R/W
0x0718 to 0x0764	***Module 2 Interrupt Vector 7-26 - Reserved***	R/W
0x0768	***Module 2 Interrupt Vector 27 - Summary***	R/W
0x076C to 0x077C	***Module 2 Interrupt Vector 28-32 - Reserved***	R/W

0x0800	***Module 2 Interrupt Steering 1 - BIT***	R/W
0x0804	***Module 2 Interrupt Steering 2 - Reserved***	R/W
0x0808	***Module 2 Interrupt Steering 3 - Strain Alert Low 1***	R/W
0x080C	***Module 2 Interrupt Steering 4 - Strain Alert Low 2***	R/W
0x0810	***Module 2 Interrupt Steering 5 - Strain Alert High 1***	R/W
0x0814	***Module 2 Interrupt Steering 6 - Strain Alert High 2***	R/W
0x0818 to 0x0864	***Module 2 Interrupt Steering 7-26 - Reserved***	R/W
0x0868	***Module 2 Interrupt Steering 27 - Summary***	R/W
0x086C to 0x087C	***Module 2 Interrupt Steering 28-32 - Reserved***	R/W

0x0900	***Module 3 Interrupt Vector 1 - BIT***	R/W
0x0904	***Module 3 Interrupt Vector 2 - Reserved***	R/W
0x0908	***Module 3 Interrupt Vector 3 - Strain Alert Low 1***	R/W
0x090C	***Module 3 Interrupt Vector 4 - Strain Alert Low 2***	R/W
0x0910	***Module 3 Interrupt Vector 5 - Strain Alert High 1***	R/W
0x0914	***Module 3 Interrupt Vector 6 - Strain Alert High 2***	R/W
0x0918 to 0x0964	***Module 3 Interrupt Vector 7-26 - Reserved***	R/W
0x0968	***Module 3 Interrupt Vector 27 - Summary***	R/W
0x096C to 0x097C	***Module 3 Interrupt Vector 28-32 - Reserved***	R/W

0x0A00	***Module 3 Interrupt Steering 1 - BIT***	R/W
0x0A04	***Module 3 Interrupt Steering 2 - Reserved***	R/W
0x0A08	***Module 3 Interrupt Steering 3 - Strain Alert Low 1***	R/W
0x0A0C	***Module 3 Interrupt Steering 4 - Strain Alert Low 2***	R/W
0x0A10	***Module 3 Interrupt Steering 5 - Strain Alert High 1***	R/W
0x0A14	***Module 3 Interrupt Steering 6 - Strain Alert High 2***	R/W
0x0A18 to 0x0A64	***Module 3 Interrupt Steering 7-26 - Reserved***	R/W
0x0A68	***Module 3 Interrupt Steering 27 - Summary***	R/W
0x0A6C to 0x0A7C	***Module 3 Interrupt Steering 28-32 - Reserved***	R/W

0x0B00	***Module 4 Interrupt Vector 1 - BIT***	R/W
0x0B04	***Module 4 Interrupt Vector 2 - Reserved***	R/W
0x0B08	***Module 4 Interrupt Vector 3 - Strain Alert Low 1***	R/W
0x0B0C	***Module 4 Interrupt Vector 4 - Strain Alert Low 2***	R/W
0x0B10	***Module 4 Interrupt Vector 5 - Strain Alert High 1***	R/W
0x0B14	***Module 4 Interrupt Vector 6 - Strain Alert High 2***	R/W
0x0B18 to 0x0B64	***Module 4 Interrupt Vector 7-26 - Reserved***	R/W
0x0B68	***Module 4 Interrupt Vector 27 - Summary***	R/W
0x0B6C to 0x0B7C	***Module 4 Interrupt Vector 28-32 - Reserved***	R/W

0x0C00	***Module 4 Interrupt Steering 1 - BIT***	R/W
0x0C04	***Module 4 Interrupt Steering 2 - Reserved***	R/W
0x0C08	***Module 4 Interrupt Steering 3 - Strain Alert Low 1***	R/W
0x0C0C	***Module 4 Interrupt Steering 4 - Strain Alert Low 2***	R/W
0x0C10	***Module 4 Interrupt Steering 5 - Strain Alert High 1***	R/W
0x0C14	***Module 4 Interrupt Steering 6 - Strain Alert High 2***	R/W
0x0C18 to 0x0C64	***Module 4 Interrupt Steering 7-26 - Reserved***	R/W
0x0C68	***Module 4 Interrupt Steering 27 - Summary***	R/W
0x0C6C to 0x0C7C	***Module 4 Interrupt Steering 28-32 - Reserved***	R/W

0x0D00	***Module 5 Interrupt Vector 1 - BIT***	R/W
0x0D04	***Module 5 Interrupt Vector 2 - Reserved***	R/W
0x0D08	***Module 5 Interrupt Vector 3 - Strain Alert Low 1***	R/W
0x0D0C	***Module 5 Interrupt Vector 4 - Strain Alert Low 2***	R/W
0x0D10	***Module 5 Interrupt Vector 5 - Strain Alert High 1***	R/W
0x0D14	***Module 5 Interrupt Vector 6 - Strain Alert High 2***	R/W
0x0D18 to 0x0D64	***Module 5 Interrupt Vector 7-26 - Reserved***	R/W
0x0D68	***Module 5 Interrupt Vector 27 - Summary***	R/W
0x0D6C to 0x0D7C	***Module 5 Interrupt Vector 28-32 - Reserved***	R/W

0x0E00	***Module 5 Interrupt Steering 1 - BIT***	R/W
0x0E04	***Module 5 Interrupt Steering 2 - Reserved***	R/W
0x0E08	***Module 5 Interrupt Steering 3 - Strain Alert Low 1***	R/W
0x0E0C	***Module 5 Interrupt Steering 4 - Strain Alert Low 2***	R/W
0x0E10	***Module 5 Interrupt Steering 5 - Strain Alert High 1***	R/W
0x0E14	***Module 5 Interrupt Steering 6 - Strain Alert High 2***	R/W
0x0E18 to 0x0E64	***Module 5 Interrupt Steering 7-26 - Reserved***	R/W
0x0E68	***Module 5 Interrupt Steering 27 - Summary***	R/W
0x0E6C to 0x0E7C	***Module 5 Interrupt Steering 28-32 - Reserved***	R/W

0x0F00	***Module 6 Interrupt Vector 1 - BIT***	R/W
0x0F04	***Module 6 Interrupt Vector 2 - Reserved***	R/W
0x0F08	***Module 6 Interrupt Vector 3 - Strain Alert Low 1***	R/W
0x0F0C	***Module 6 Interrupt Vector 4 - Strain Alert Low 2***	R/W
0x0F10	***Module 6 Interrupt Vector 5 - Strain Alert High 1***	R/W
0x0F14	***Module 6 Interrupt Vector 6 - Strain Alert High 2***	R/W
0x0F18 to 0x0F64	***Module 6 Interrupt Vector 7-26 - Reserved***	R/W
0x0F68	***Module 6 Interrupt Vector 27 - Summary***	R/W
0x0F6C to 0x0F7C	***Module 6 Interrupt Vector 28-32 - Reserved***	R/W

0x1000	***Module 6 Interrupt Steering 1 - BIT***	R/W
0x1004	***Module 6 Interrupt Steering 2 - Reserved***	R/W
0x1008	***Module 6 Interrupt Steering 3 - Strain Alert Low 1***	R/W
0x100C	***Module 6 Interrupt Steering 4 - Strain Alert Low 2***	R/W
0x1010	***Module 6 Interrupt Steering 5 - Strain Alert High 1***	R/W
0x1014	***Module 6 Interrupt Steering 6 - Strain Alert High 2***	R/W
0x1018 to 0x1064	***Module 6 Interrupt Steering 7-26 - Reserved***	R/W
0x1068	***Module 6 Interrupt Steering 27 - Summary***	R/W
0x106C to 0x107C	***Module 6 Interrupt Steering 28-32 - Reserved***	R/W

APPENDIX: PIN-OUT DETAILS

Pin-out details (for reference) are shown below, with respect to DATAIO. Additional information on pin-outs can be found in the Motherboard Operational Manuals.

Module Signal (Ref Only)	Strain Gauge (SG1)
DATIO1	BRG-H-CH1
DATIO2	BRG-L-CH1
DATIO3	DRV-H-SNS-CH1
DATIO4	DRV-L-SNS-CH1
DATIO5	DRV-H-CH1
DATIO6	DRV-L-CH1
DATIO7	BRG-H-CH2
DATIO8	BRG-L-CH2
DATIO9	DRV-H-SNS-CH2
DATIO10	DRV-L-SNS-CH2
DATIO11	DRV-H-CH2
DATIO12	DRV-L-CH2
DATIO13	BRG-H-CH3
DATIO14	BRG-L-CH3
DATIO15	DRV-H-SNS-CH3
DATIO16	DRV-L-SNS-CH3
DATIO17	DRV-H-CH3
DATIO18	DRV-L-CH3
DATIO19	BRG-H-CH4
DATIO20	BRG-L-CH4
DATIO21	DRV-H-SNS-CH4
DATIO22	DRV-L-SNS-CH4
DATIO23	DRV-H-CH4
DATIO24	DRV-L-CH4
DATIO25	BRG-L-COMP-CH1
DATIO26	
DATIO27	BRG-L-COMP-CH2
DATIO28	
DATIO29	BRG-L-COMP-CH3
DATIO30	
DATIO31	BRG-L-COMP-CH4
DATIO32	
DATIO33	
DATIO34	
DATIO35	
DATIO36	
DATIO37	
DATIO38	
DATIO39	
DATIO40	
N/A	




Status and Interrupts

MODULE MANUAL

STATUS AND INTERRUPTS

Status registers indicate the detection of faults or events. The status registers can be channel bit-mapped or event bit-mapped. An example of a channel bit-mapped register is the BIT status register, and an example of an event bit-mapped register is the FIFO status register.

For those status registers that allow interrupts to be generated upon the detection of the fault or the event, there are four registers associated with each status: *Dynamic, Latched, Interrupt Enabled*, and *Set Edge/Level Interrupt*.

Dynamic Status: The *Dynamic Status* register indicates the *current* condition of the fault or the event. If the fault or the event is momentary, the contents in this register will be clear when the fault or the event goes away. The *Dynamic Status* register can be polled, however, if the fault or the event is sporadic, it is possible for the indication of the fault or the event to be missed.

Latched Status: The *Latched Status* register indicates whether the fault or the event *has occurred* and keeps the state until it is cleared by the user. Reading the *Latched Status* register is a better alternative to polling the *Dynamic Status* register because the contents of this register will not clear until the user commands to clear the specific bit(s) associated with the fault or the event in the *Latched Status* register. Once the status register has been read, the act of writing a **1** back to the applicable status register to any specific bit (channel/event) location will "clear" the bit (set the bit to **0**). When clearing the channel/event bits, it is strongly recommended to write back the same bit pattern as read from the *Latched Status* register. For example, if the channel bit-mapped *Latched Status* register contains the value 0x0000 0005, which indicates fault/event detection on channel 1 and 3, write the value 0x0000 0005 to the *Latched Status* register to clear the fault/event status for channel 1 and 3. Writing a "1" to other channels that are not set (example 0x0000 000F) may result in incorrectly "clearing" incoming faults/events for those channels (example, channel 2 and 4).

Interrupt Enable: If interrupts are preferred upon the detection of a fault or an event, enable the specific channel/event interrupt in the *Interrupt Enable* register. The bits in *Interrupt Enable* register map to the same bits in the *Latched Status* register. When a fault or event occurs, an interrupt will be fired. Subsequent interrupts will not trigger until the application acknowledges the fired interrupt by clearing the associated channel/event bit in the *Latched Status* register. If the interruptible condition is still persistent after clearing the bit, this may retrigger the interrupt depending on the *Edge/Level* setting.

Set Edge/Level Interrupt: When interrupts are enabled, the condition on retriggering the interrupt after the Latch Register is "cleared" can be specified as "edge" triggered or "level" triggered. Note, the Edge/Level Trigger also affects how the Latched Register value is adjusted after it is "cleared" (see below).

- *Edge triggered*: An interrupt will be retriggered when the Latched Status register change from low (0) to high (1) state. Uses for edge-triggered interrupts would include transition detections (Low-to-High transitions, High-to-Low transitions) or fault detections. After "clearing" an interrupt, another interrupt will not occur until the next transition or the re-occurrence of the fault again.
- *Level triggered*: An interrupt will be generated when the Latched Status register remains at the high (1) state. Level-triggered interrupts are used to indicate that something needs attention.

Interrupt Vector and Steering

When interrupts are enabled, the interrupt vector associated with the specific interrupt can be programmed with a unique number/identifier defined by the user such that it can be utilized in the Interrupt Service Routine (ISR) to identify the type of interrupt. When an interrupt occurs, the contents of the Interrupt Vector registers is reported as part of the interrupt mechanism. In addition to specifying the interrupt vector, the interrupt can be directed ("steered") to the native bus or to the application running on the onboard ARM processor.

Interrupt Trigger Types

In most applications, limiting the number of interrupts generated is preferred as interrupts are costly, thus choosing the correct Edge/Level interrupt trigger to use is important.

Example 1: Fault detection

This example illustrates interrupt considerations when detecting a fault like an “open” on a line. When an “open” is detected, the system will receive an interrupt. If the “open” on the line is persistent and the trigger is set to “edge”, upon “clearing” the interrupt, the system will not re-generate another interrupt. If, instead, the trigger is set to “level”, upon “clearing” the interrupt, the system will re-generate another interrupt. Thus, in this case, it will be better to set the trigger type to “edge”.

Example 2: Threshold detection

This example illustrates interrupt considerations when detecting an event like reaching or exceeding the “high watermark” threshold value. In a communication device, when the number of elements received in the FIFO reaches the high-watermark threshold, an interrupt will be generated. Normally, the application would read the count of the number of elements in the FIFO and read this number of elements from the FIFO. After reading the FIFO data, the application would “clear” the interrupt. If the trigger type is set to “edge”, another interrupt will be generated only if the number of elements in FIFO goes below the “high watermark” after the “clearing” the interrupt and then fills up to reach the “high watermark” threshold value. Since receiving communication data is inherently asynchronous, it is possible that data can continue to fill the FIFO as the application is pulling data off the FIFO. If, at the time the interrupt is “cleared”, the number of elements in the FIFO is at or above the “high watermark”, no interrupts will be generated. In this case, it will be better to set the trigger type to “level”, as the purpose here is to make sure that the FIFO is serviced when the number of elements exceeds the high watermark threshold value. Thus, upon “clearing” the interrupt, if the number of elements in the FIFO is at or above the “high watermark” threshold value, another interrupt will be generated indicating that the FIFO needs to be serviced.

Dynamic and Latched Status Registers Examples

The examples in this section illustrate the differences in behavior of the Dynamic Status and Latched Status registers as well as the differences in behavior of Edge/Level Trigger when the Latched Status register is cleared.

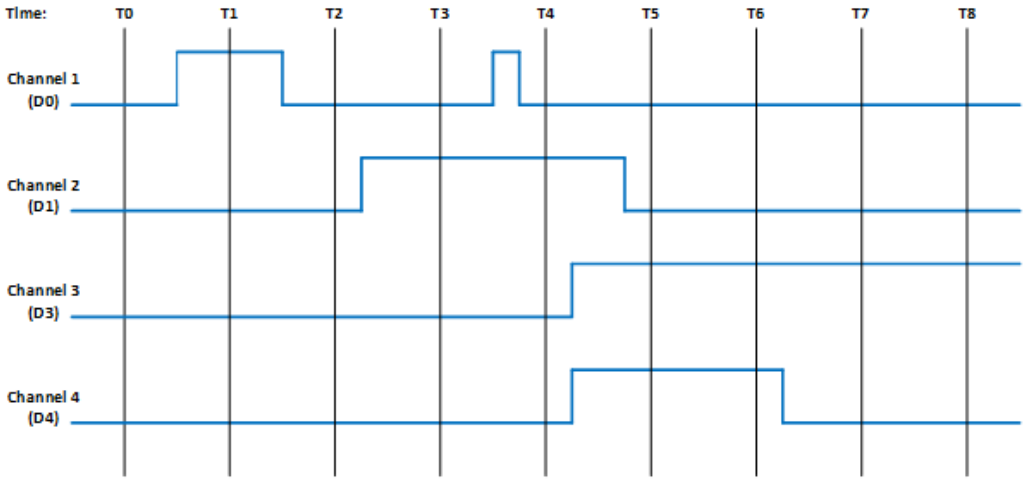


Figure 1. Example of Module's Channel-Mapped Dynamic and Latched Status States

Time	Dynamic Status	No Clearing of Latched Status	Clearing of Latched Status (Edge-Triggered)		Clearing of Latched Status (Level-Triggered)	
		Latched Status	Action	Latched Status	Action	Latched
T0	0x0	0x0	Read Latched Register	0x0	Read Latched Register	0x0
T1	0x1	0x1	Read Latched Register	0x1		0x1
			Write 0x1 to Latched Register		Write 0x1 to Latched Register	
				0x0		*0x1*
T2	0x0	0x1	Read Latched Register	0x0	Read Latched Register	0x1
					Write 0x1 to Latched Register	
						0x0
T3	0x2	0x3	Read Latched Register	0x2	Read Latched Register	0x2
			Write 0x2 to Latched Register		Write 0x2 to Latched Register	
				0x0		*0x2*
T4	0x2	0x3	Read Latched Register	0x1	Read Latched Register	0x3
			Write 0x1 to Latched Register		Write 0x3 to Latched Register	
				0x0		*0x2*
T5	0xC	0xF	Read Latched Register	0xC	Read Latched Register	0xE
			Write 0xC to Latched Register		Write 0xE to Latched Register	
				0x0		*0xC*
T6	0xC	0xF	Read Latched Register	0x0	Read Latched Register	0xC
					Write 0xC to Latched Register	
						0xC
T7	0x4	0xF	Read Latched Register	0x0	Read Latched Register	0xC
					Write 0xC to Latched Register	
						0x4
T8	0x4	0xF	Read Latched Register	0x0	Read Latched Register	0x4

Interrupt Examples

The examples in this section illustrate the interrupt behavior with Edge/Level Trigger.

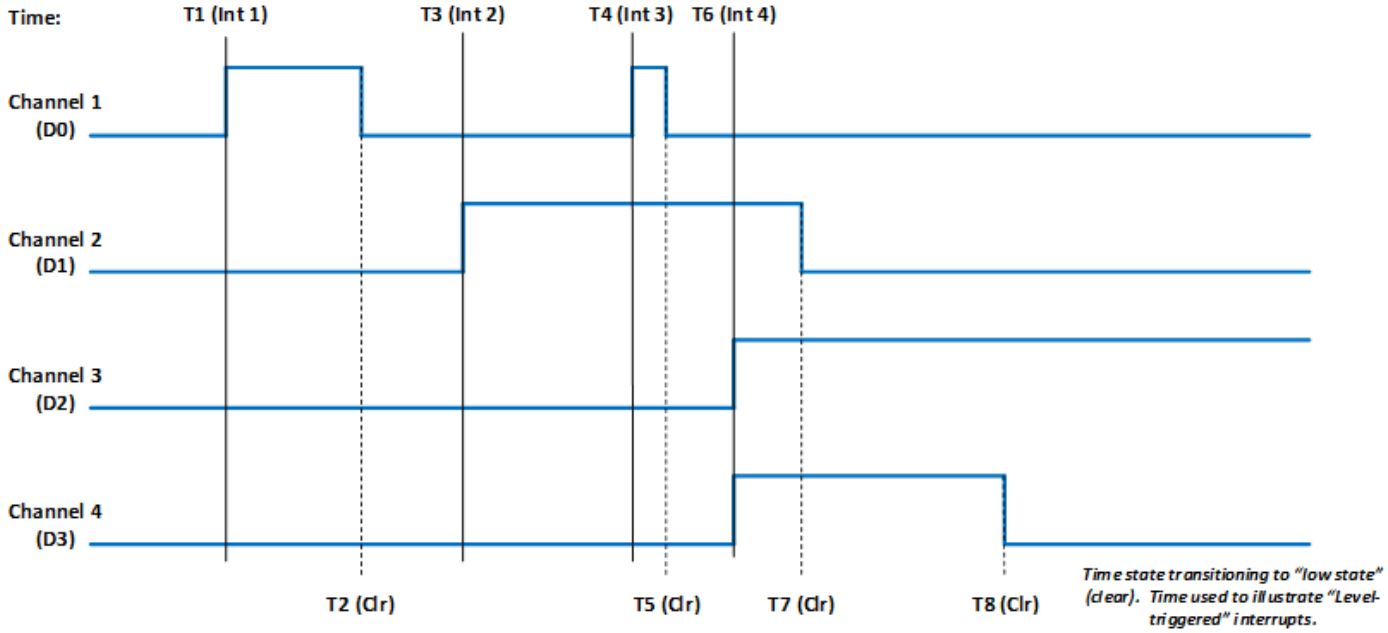


Figure 2. Illustration of Latched Status State for Module with 4-Channels with Interrupt Enabled

Time	Latched Status (Edge-Triggered – Clear Multi-Channel)		Latched Status (Edge-Triggered – Clear Single Channel)		Latched Status (Level-Triggered – Clear Multi-Channel)	
	Action	Latched	Action	Latched	Action	Latched
T1 (Int 1)	**Interrupt Generated** Read Latched Registers	0x1	**Interrupt Generated** Read Latched Registers	0x1	**Interrupt Generated** Read Latched Registers	0x1
	Write 0x1 to Latched Register		Write 0x1 to Latched Register		Write 0x1 to Latched Register	
		0x0		*0x0*	***Interrupt re-triggers*** Note, interrupt re-triggers after each clear until T2.	*0x1*
T3 (Int 2)	**Interrupt Generated** Read Latched Registers	0x2	**Interrupt Generated** Read Latched Registers	0x2	**Interrupt Generated** Read Latched Registers	0x2
	Write 0x2 to Latched Register		Write 0x2 to Latched Register		Write 0x2 to Latched Register	
		0x0		*0x0*	***Interrupt re-triggers*** Note, interrupt re-triggers after each clear until T7.	*0x2*
T4 (Int 3)	**Interrupt Generated** Read Latched Registers	0x1	**Interrupt Generated** Read Latched Registers	0x1	**Interrupt Generated** Read Latched Registers	0x3
	Write 0x1 to Latched Register		Write 0x1 to Latched Register		Write 0x3 to Latched Register	
		0x0		*0x0*	***Interrupt re-triggers*** Note, interrupt re-triggers after each clear and 0x3 is reported in Latched Register until T5.	*0x3*
					Interrupt re-triggers Note, interrupt re-triggers after each clear until T7.	*0x2*

Time	Latched Status (Edge-Triggered – Clear Multi-Channel)		Latched Status (Edge-Triggered – Clear Single Channel)		Latched Status (Level-Triggered – Clear Multi-Channel)	
	Action	Latched	Action	Latched	Action	Latched
T6 (Int 4)	**Interrupt Generated** Read Latched Registers	0xC	**Interrupt Generated** Read Latched Registers	0xC	**Interrupt Generated** Read Latched Registers	0xE
	Write 0xC to Latched Register		Write 0x4 to Latched Register		Write 0xE to Latched Register	
		0x0	***Interrupt re-triggers*** Write 0x8 to Latched Register	*0x8*	***Interrupt re-triggers*** Note, interrupt re-triggers after each clear and 0xE is reported in Latched Register until T7.	*0xE*
				0x0	***Interrupt re-triggers*** Note, interrupt re-triggers after each clear and 0xC is reported in Latched Register until T8.	*0xC*
					Interrupt re-triggers Note, interrupt re-triggers after each clear and 0x4 is reported in Latched Register always.	*0x4*

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